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Applicant(s) <b>A. Watson, et al.</b>	
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**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE



**U.S. PATENT APPLICATION PUBLICATIONS**

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**FOREIGN PATENT DOCUMENTS**

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
<i>RD</i>		JP2020039	01/23/1990	Japan		abstract	✓	

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>RD</i>		SUBSTRATE MODELING AND LUMPED SUBSTRATE RESISTANCE EXTRACTION FOR CMOS ESD/LATCHUP CIRCUIT SIMULATION, T. Li, et al., Coordinated Science Laboratory, Dept. of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, Urbana, IL (1999), 6 pages; 1999 ACM.
<i>RD</i>		BIPOLAR TRANSISTOR ACTION AND TRANSPORT EFFECTS RELATING TO CMOS LATCHUP, G. Krieger, IEEE Transactions on Electron Devices, Vol. ED-34, No. 8, August 1987, pgs. 1719-1728

EXAMINER <i>Phellaker Kik</i>	DATE CONSIDERED <i>6/24/06</i>
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